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Applicant: SONY CORPORATION 7-35, Kitashinagawa 6-chome Shinagawa-ku Tokyo(JP)

inventor: Ueki, Masaaki
c/o Sony Corporation 7-35 Kitashinagawa
6-chome
Shinagawa-ku Tokyo(JP)

Shinagawa-ku Tokyo(JP) Inventor: Yasuda, Nobuyuki

c/o Sony Corporation 7-35 Kitashinagawa

6-chome

Shinagawa-ku Tokyo(JP) Inventor: Masuda, Toshihiko

c/o Sony Corporation 7-35 Kitashinagawa

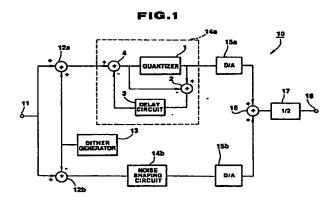
6-chome

Shinagawa-ku Tokyo(JP)

Representative: Ayers, Martyn Lewis Stanley et al J.A. KEMP & CO. 14 South Square Gray's Inn London, WC1R 5EU(GB)

(S4) Signal processing apparatus.

(57) A signal processing apparatus for reducing the quantisation noise by using two or more so-called noise shaping circuits (14a, 14b), is disclosed. The input signal may be audio or video signals. One of the noise shaping circuits (14a) is supplied with a signal which is the relative addition of the input Signal and the dither while the other noise shaping Circuit (14b) is supplied with a signal which is the relative subtraction of the input signal and the dither. The signal components of the outputs of the noise shaping circuits are effectively combined together to cancel the dither components to produce an output with an improved S/N ratio. A plurality of such signal processing apparatus may also be arranged in parallel (see figure 5), in which case different dithers are used in the respective signal processing apparatus and the outputs of the respective signal processing apparatus are combined to further improve the S/N ratio.



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SIGNAL PROCESSING APPARATUS

This invention relates to a signal processing apparatus which makes use of a so-called noise shaping circuit to reduce the quantisation noise.

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Noise shaping is a technology according to which the spectrum of quantisation noise produced at the time of quantising or rounding data such as audio or video signal data is changed so that, for example, the noise level in the audio range is reduced significantly to improve the signal to noise (S/N) ratio. A known technique for noise shaping involves feeding back quantisation error components to the input side, as disclosed for example in "Adaptive Noise Spectral Shaping and Entropy Coding in Predictive Coding of Speech" appearing in IEEE Transactions on Acoustics, Speech and Processing, February 1979, volume ASSP-27, No 1, pages 63 to 73. However, when an audio signal, for example, is subjected to such noise shaping, a characteristic pattern, the so-called "idling pattern", which is rather harsh to the ear, may be produced at minute signal levels.

The conventional practice to overcome this difficulty is to perform noise shaping after a dither signal is added to an input signal, as disclosed in the Japanese laid open patent publication number 51-48214, and as shown herein in figure 6.

In this figure, an input signal supplied to an input terminal 61 is supplied to an adder 62 where there is added to it a dither signal from a dither generator 63, the sum of these two then applied to a noise shaping circuit 64. The output from the noise shaping circuit 64 is transmitted to a D/A converter 65 and thereby converted into corresponding analog signals which are output from an output terminal 68.

Figure 7 shows the frequency spectrum of the output signals from an output terminal 68. In this figure, X stands for an input signal, D a dither signal introduced at the input side and V_N a quantisation error component. By noise shaping, the quantisation noise component V_N exhibits a lower noise level at the lower frequencies in the audio range. The output signal Y from the output terminal 68 is represented by the following formula (1)

$$Y = X + S + V_N \qquad (1)$$

Hence, difficulty arises that the dither signal D is outputted even though there is no input signal, that is the input signal X is zero. The signal to quantisation noise power ratio or S/N ratio is given by the formula (2)

$$S/N = X^2/V_N 2 \qquad (2)$$

It is also necessary that the frequency range of the introduced dither signal lies outside the audio range, while it is also necessary that the dither signal remaining at the time of D/A conversion be removed by a low pass filter.

It is an object of the present invention to obviate the above difficulties of the prior art and to provide a signal processing apparatus according to which a dither signal component in the output signal which is obtained by introducing a dither signal into an input signal and noise shaping the resulting mixed signal may be cancelled by a simplified system.

It is another object of the present invention to provide a signal processing apparatus whereby the signal to quantisation noise ratio or S/N ratio may be further improved.

According to the present invention, there is provided a signal processing apparatus adapted for reducing the quantisation noise generated at the time of quantising data comprising an input terminal to which, in use, an input signal is supplied,

a dither generator for generating a dither,

a first noise shaping circuit to which, in use, a signal representing relative addition between said input signal and said dither is supplied,

a second noise shaping circuit to which, in use, a signal representing relative subtraction between said input signal and said dither is supplied, and combining means for effectively combining respective components of output signals of said first and second noise shaping circuits.

The invention also provides a signal processing apparatus comprising a plurality of signal processing circuits to each of which, in use, an input signal is supplied in parallel, each of said signal processing circuit comprising

a dither generator for generating a dither,

a first noise shaping circuit to which, in use, a signal representing relative addition between said input signal and said dither is supplied,

a second noise shaping circuit to which, in use, a signal representing relative subtraction between said input signal and said dither is supplied, and combining means for effectively combining respective components of output signals of said first and second noise shaping circuits,

the outputs of said signal processing circuits being combined together.

Thus, at least two noise shaping circuits are employed. One of the noise shaping circuits is supplied with the sum of the dither signal and the input signal while the other noise shaping circuit is supplied with a difference signal between the dither signal and the input signal. The output signals from the noise shaping circuits are summed together or subtracted one from the other so that the respective input signal components are effectively

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summed together while the dither signal components are cancelled.

Therefore, at the final stage of signal addition or subtraction, the dither signal components in the output signals are cancelled by signal subtraction and the input signal components are doubled in amplitude and squared in power by signal addition, whereas the quantisation noise components in the output signals are simply doubled in power, resulting in an improved S/N ratio.

The invention will be further described by way of non-limitative example with reference to the accompanying drawings, in which:-

Figure 1 is a block circuit diagram showing a first embodiment of a signal processing apparatus according to the present invention.

Figure 2 is a chart showing the frequency spectrum of an output signal in the embodiment shown in figure 1.

Figure 3 is a block circuit diagram showing a second embodiment of a signal processing apparatus according to the present invention.

Figure 4 is a block circuit diagram showing a third embodiment of a signal processing apparatus according to the present invention.

Figure 5 is a block circuit diagram showing a fourth embodiment of a signal processing apparatus according to the present invention.

Figure 6 is a block circuit diagram showing a conventional signal processing apparatus.

Figure 7 is a chart showing the frequency diagram of an output signal of the apparatus shown in figure 6.

In the drawings, like reference numerals are used to denote like parts or parts performing like functions.

Figure 1 shows, in a block circuit diagram, a first embodiment of a signal processing apparatus according to the present invention.

In the signal processing apparatus 10, shown in figure 1, a digital audio signal composed of, for example, 16 bits, is supplied to an input terminal 11 and thence to adders 12a and 12b. A dither signal from a dither generator 13 is added to the input signal at an adder 12a and the resulting sum signal is supplied to a noise shaping circuit 14a. The dither signal from the dither generator 13 is subtracted from the input signal at an adder 12b and the resulting difference signal is supplied to a noise shaping circuit 14b. The noise shaping circuits 14a, 14b may effect substantially identical noise shaping of their inputs and may be of the same construction. Specifically they may be of a type in which quantisation errors produced when reducing the number of bits of the input digital signal by a quantiser or requantiser, for example, rounding a 16-bit input to a 4-bit output, are fed back to the input side, by way of an error feedback operation. That is, the noise shaping circuit 14a or 14b is so arranged and constructed that an input to a quantiser 1 is subtracted from an output to the quantiser 1 by an adder 2 and the resulting subtraction output or quantisation error is fed back to an input side adder 4 of the quantiser 1 by way of a delay circuit 3. The outputs from these noise shaping circuits 14a and 14b are transmitted to D/A converters 15a and 15b, respectively, where they are converted into corresponding analog signals which are then combined together at an adder 16 and attenuated in gain by the half by a 1/2 attenuator before being taken out at an output terminal 18.

In the above described signal processing apparatus 10, the dither signal D from the dither generator 13 is added to the input signal X to the input terminal 11 at the adder 12a, while it is subtracted from the input signal at the other adder 12b, and the resulting sum and subtraction signals are subjected separately to noise shaping. Thus an output signal Y_1 of an addition system and an output signal Y_2 of a subtraction system may be represented by the formulae (3) and (4)

$$Y_1 = X + D + V_N$$
 (3)
 $Y_2 = X - D + V_N$ (4)

respectively, where V and V_N are quantisation noises at the noise shaping circuits 14a and 14b, respectively. These signals Y_1 and Y_2 are combined together at the adder 16 to cancel the dither signal D completely. The input signal becomes 2X by such addition, that is the amplitude is doubled, so that the power is equal to $(2X)^2$. On the other hand, the quantisation noises V_N and V_N are of a random phase, so that the noise power after the above addition is equal to $V_N 2 + V_N 2$ and, if the noises are of equal amplitude, the noise power is equal to $2V_N 2$. Hence the power ratio of the signal component to the quantisation noise or S/N ratio is given by the formula (5)

S/N =
$$4X^2/2V_N2 = 2(X^2/V_N2)$$
 (5) which means that the S/N ratio is twice that of the prior art system indicated by the formula (2), that is, the S/N ratio is improved by 3 decibels (dB). Figure 2 shows the frequency spectrum of the output signal following such addition. The broken line in figure 2 illustrates, for reference sake, the frequency spectrum in the prior art which by itself is shown in figure 7.

Also, since the dither signal introduced at the input side has been cancelled in the ultimate output signal, the dither signal, which it has hitherto been thought impossible to superimpose in the audio range, can now be superimposed in the audio range. For example, an M-series random number signal, which is not subject to bandwidth limitation, may be used as the dither signal.

Figure 3 shows a second embodiment of the

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present invention in which the D/A conversion of the first embodiment is performed at the last stage.

In the signal processing circuit 20, shown in figure 3, the input signal supplied to an input terminal 21 is transmitted therefrom to adders 22a and 22b where dither signals from a dither generator 13 are added to or subtracted from the input signal and the resulting sum and difference signals are supplied to noise shaping circuit 24a and 24b respectively. The outputs from these noise shaping circuits 24a and 24b are combined together in advance at an adder 26 where the dither signal components are cancelled and the input signal components are combined together. The output from the adder 26 is attenuated by 1/2 by a 1/2 attenuator 27 and the attenuated signal is transmitted to a D/A converter 25 for D/A conversion before being taken out at an output terminal 28.

The second embodiment is similar in operation and result to the above described first embodiment and, besides, is more economically advantageous since only one D/A converter suffices.

By way of a modification of either of the above embodiments, input signals having opposite polarities or phases may be superimposed on a dither signal of the same polarity or phase and signal subtraction may be performed after noise shaping.

Thus, in a signal processing circuit 30 according to a third embodiment, shown in figure 4, an input signal supplied to an input terminal 31 is supplied to an adder 32a while being inverted in polarity or phase by an inverter 39 and supplied to an adder 32b. in these adders 32a and 32b, the dither signal from the dither generator 33 is added to the non-inverted input signal and to the inverted input signal, respectively. Since the input signals are reversed in polarity, or phase, relative to each other, the input signals and the dither signals are subjected to addition on one hand and to relative subtraction on the other. The outputs from these adders 32a and 32b are transmitted to noise shaping circuits 34a and 34b, respectively and thence to D/A converters 35a and 35b, respectively, so as to be converted into corresponding signals which are supplied to an adder 36. In the adder 36, one of the signals is subtracted from the other, thus so that the input signal components having the opposite polarity or phase to each other are combined together. The output from the adder 36 is attenuated in gain by 1/2 by a 1/2 attenuator 37 before being taken out at an output terminal 38.

It is to be noted that the present third embodiment operates and produces a result similar to that of the above described first embodiment. In the present third embodiment, the outputs from the noise shaping circuits 34a and 34b may be subjected to subtraction at an adder and the resulting difference signal may then be converted into a

corresponding signal by one D/A converter, similarly to the above described second embodiment.

The above description has been made of an example of using two noise shaping circuits. Alternatively, provision may be made of an n number of signal processing circuits, each having two noise shaping circuits, and an n number of different dither signals may be used in the signal processing circuits.

Thus, according to a fourth embodiment, shown in figure 5, each of circuits 10₁, 10₂, ..., 10_n is the same as the signal processing apparatus 10 of the above described first embodiment and different dither signals are used in the respective circuits 10, to 10_n. An input signal from an input terminal 41 is supplied to each of these circuits 10, to 10_n. The output signals from these circuits 10₁ to 10_n are supplied to an adder 42 and thence to a 1/n attenuator 43 where the output signal of the adder 42 is attenuated by 1/n before being taken out at an output terminal 44. As these circuits 101 to 10_n, the signal processing circuits 20 or 30 may be used either alone or in combination. It is however necessary to use different dither signals for the circuits 10₁ to 10_n.

In the fourth embodiment, shown in figure 5, the S/N ratio of the output signal at the output terminal 44 is improved further and by 3 x log₂n decibels (dB).

According to the signal processing apparatus of the present invention, dither signal components in the output signal may be cancelled completely so that the necessity of providing an analog LPF, for example, for D/A conversion, may be eliminated to simplify the circuitry, while the signals not placed under bandwidth limitations, such as M series signals, may be used as the dither signals. The signal to noise ratio may also be improved since the input signal components in the noise shaping circuit outputs are effectively summed together at the final stage of signal processing.

Claims

1. A signal processing apparatus adapted for reducing the quantisation noise generated at the time of quantising data comprising

an input terminal (11) to which, in use, an input signal is supplied,

a dither generator (13) for generating a dither,

a first noise shaping circuit (14a) to which, in use, a signal representing relative addition between said input signal and said dither is supplied,

a second noise shaping circuit (14b) to which, in use, a signal representing relative subtraction between said input signal and said dither is supplied, and

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combining means (16) for effectively combining respective components of output signals of said first and second noise shaping circuits (14a, 14b).

- 2. The signal processing apparatus according to claim 1 wherein each said noise shaping circuit (14a, 14b) comprises
- a quantiser (1),
- a first subtractor (2) for subtracting an input signal to said quantiser (1) from an output signal from said quantiser (1), and
- a second subtractor (4) for subtracting a delayed output signal of said first subtractor (1) from said input signal to said quantiser.
- 3. The signal processing apparatus according to claim 1 or 2 wherein
- a signal which is the sum of said input signal and said dither is supplied to said first noise shaping circuit (14a), and wherein
- a signal which is the sum of an inversion of said input signal and said dither is supplied to said second noise shaping circuit (14b).
- 4. The signal processing apparatus according to claim 3 in which the combining means comprises a subtractor (36) for subtracting outputs of said first and second noise shaping circuits one from the other.
- 5. The signal processing apparatus according to any one of the preceding claims further comprising a D/A converter (25, 35) to which the output of said combining means is supplied.
- 6. A signal processing apparatus comprising a plurality of signal processing circuits (10_1 , 10_2 , ... 10_n) to each of which, in use, an input signal is supplied in parallel, each of said signal processing circuit comprising
- a dither generator (33) for generating a dither,
- a first noise shaping circuit (14a) to which, in use, a signal representing relative addition between said input signal and said dither is supplied,
- a second noise shaping circuit (14b) to which, in use, a signal representing relative subtraction between said input signal and said dither is supplied,
- combining means (42) for effectively combining respective components of output signals of said first and second noise shaping circuits,
- the outputs of said signal processing circuits (10_1 , ... 10_n) being combined together.
- 7. The signal processing apparatus according to claim 6 wherein different dithers generated by said dither generators are used in said signal processing circuit.
- 8. The signal processing apparatus according to claim 6 or 7 comprising an N number of said signal processing circuits $(10_1, \dots 10_n)$ and gain control means (43) for attenuating the outputs of said combining means by 1/N.

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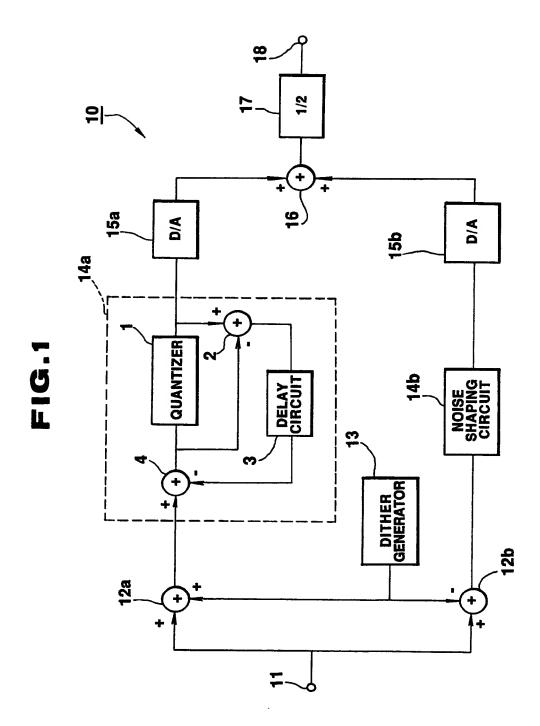
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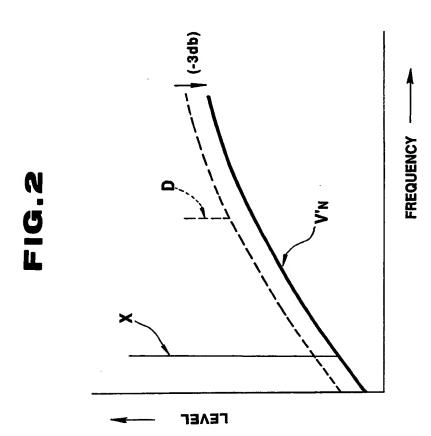
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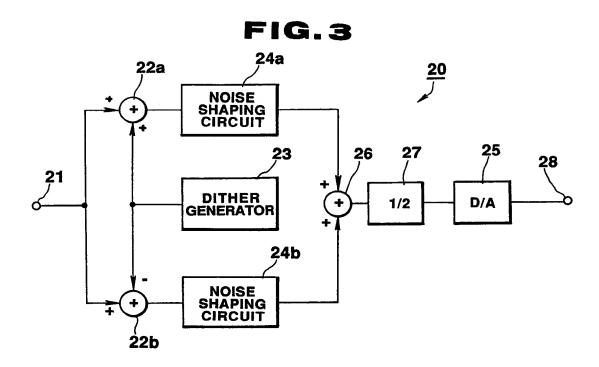


FIG.4 34a 35a 32a <u>30</u> NOISE SHAPING CIRCUIT D/A **33** 31 DITHER GENERATOR 36 34b NOISE SHAPING CIRCUIT D/A 32b **35b**

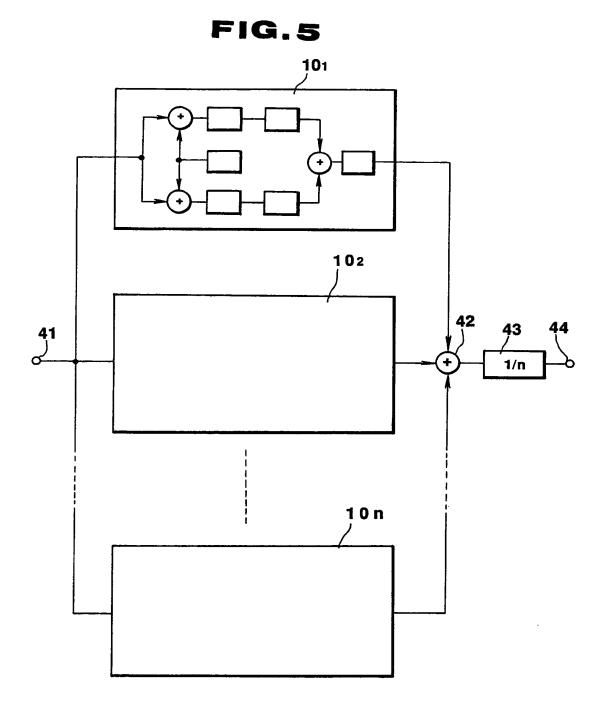


FIG.6

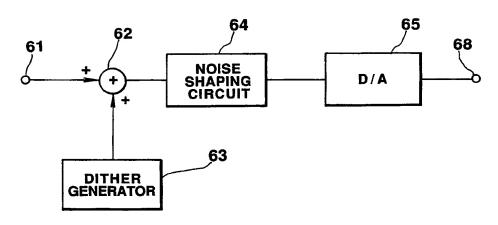
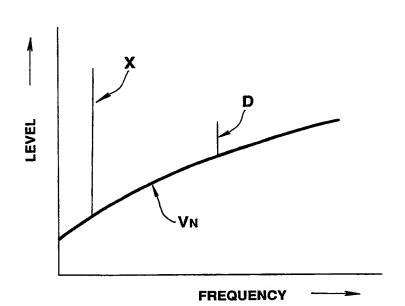


FIG.7







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7-35, Kitashinagawa 6-chome Shinagawa-ku
Tokyo(JP)

Inventor: Ueki, Masaaki

c/o Sony Corporation 7-35 Kitashinagawa

6-chome

Shinagawa-ku Tokyo(JP) Inventor: Yasuda, Nobuyuki

c/o Sony Corporation 7-35 Kitashinagawa

6-chome

Shinagawa-ku Tokyo(JP) Inventor: Masuda, Toshihiko

c/o Sony Corporation 7-35 Kitashinagawa

6-chome

Shinagawa-ku Tokyo(JP)

Representative: Ayers, Martyn Lewis Stanley et al

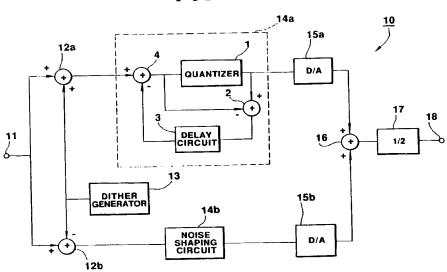
J.A. KEMP & CO. 14 South Square Gray's Inn London, WC1R 5EU(GB)

(S) Signal processing apparatus.

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shaping circuits are effectively combined together to cancel the dither components to produce an output with an improved S/N ratio. A plurality of such signal processing apparatus may also be arranged in parallel (see figure 5), in which case different dithers are used in the respective signal processing apparatus and the outputs of the respective signal processing apparatus are combined to further improve the S/N ratio.

FIG.1





EUROPEAN SEARCH REPORT

Application Number

EP 89 31 1158

DOCUMENTS CONSIDERED TO BE RELEVANT					
Category		ith indication, where appropriate, evant passages		elevant o claim	CLASSIFICATION OF THE APPLICATION (Int. CI.5)
Α	DE-A-2 341 172 (SIEMEN * page 2, line 13 - page 4, l		1		H 04 B 14/04
D,A	IEEE TRANSACTIONS ON SIGNAL PROCESSING vol YORK pages 63 - 73; MAK Spectral Shaping and Entro of Speech' * page 64, right column, line 89311158030	. 27, no. 1, February 1979, HOUL ET AL: 'Adaptive No opy Coding in Predictive Co	NEW ise	2	
					TECHNICAL FIELDS SEARCHED (Int. CI.5)
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